REMARKS

In the Office Action dated May 6, 2004, claims 1-25 were presented for examination. Claims 1-25 were rejected under 35 U.S.C. §102(b).

Applicant wishes to thank the Examiner for the careful and thorough review and action on the merits in this application. The following remarks are provided in support of the pending claims and responsive to the Office Action of May 6, 2004 for the pending application.

I. Rejection of claims 1-25 under 35 U.S.C. §102(b)

Claims 1-25 were rejected under 35 U.S.C. §102(b) as being anticipated by *Hagersten*, U.S. Patent No. 5,749,095. The *Hagersten* patent '095 relates to performing efficient write operations in a multiprocessor computer system. More specifically, *Hendersen* discloses performing write operations prior to completion of a coherency operation if the write operation includes a specific predefined code. The write operations that includes the specific predefined code are ordered with respect to each other, but not other operations performed by the processor. Col. 8, lines 10-12. *Hagersten* does not show executing local memory operation in an arbitrary order. Rather, *Hagersten* shows a method for ordering write operations that include a specific predefined code, which is not arbitrarily ordering execution of local memory operations. Accordingly, the ordering of write operations of *Hendersen* operate under different parameters and a different environment than that claimed by Applicant.

Applicant's invention applies to local memory, not cache hardware, and allowing operations associated with local memory to be executed in an arbitrary order. The Examiner notes items 18A and 18B in *Hendersen* as local memory that is allowed to execute in an arbitrary order. However, as noted in *Hendersen*, items 18A and 18B are external cache not local memory, and item 22 is designated as memory. "[e]xternal caches 18 are labeled as L2 caches (for level 2, wherein the internal caches are level 1 caches) . . .. It is noted that the "level" nomenclature is used to identify proximity of a particular cache to the processing core within

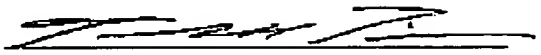
processor 16." Col. 8, lines 57-62. In addition, operations in cache are generally not allowed to execute in arbitrary order. Although *Hendersen* allows write instructions with a specific code to be executed without constraints, write instructions without the specific code must obey constraints. There is no teaching in *Henderson* for allowing an arbitrary order of execution of local memory operations. In order for the claimed invention to be anticipated under 35 U.S.C. §102(b), the prior art must teach all claimed limitations presented by the claimed invention. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." MPEP §2131 (citing *Verdegaal Bros. v. Union Oil Co. of California*, 814 F. 2d 628, 631, 2 U.S.P.Q. 2d 1051, 1053 (Fed. Cir. 1987)). As mentioned above, *Henderson* does not show all of the elements as claimed by Applicant in pending claims 1-25. Specifically, *Hendersen* does not support the use of arbitrarily ordering local memory operations, as shown in Applicant's pending claims, rather *Hendersen* shows support for changing the order of an operation associated with L2 cache. Accordingly, *Hendersen* clearly fails to teach the limitations pertaining to the execution of local memory operations as presented in Applicant's pending claims 1-25.

Finally, "[a] previous patent anticipates a purported invention only where, except for insubstantial differences, it contains all of the same elements operating in the same fashion to perform an identical function." *Saunders v. Air-Flo Co.*, 646 F.2d 1201, 1203 (7th Cir. 1981) citing *Popeil Brothers, Inc. v. Schick Electric, Inc.*, 494 F. 2d 162, 164 (7th Cir. 1974) (holding patents were not invalid as being anticipated by or obvious in light of prior art). *Hendersen* does not anticipate the invention of Applicant based upon the legal definition of anticipation. Although the prior art cited by the Examiner relates to changing the order of write operations in a multiprocessor system, *Hendersen* fails to show each and every element as presented in Applicant's claimed invention. Specifically, *Hendersen* does not show arbitrarily changing the order of local memory operations, as noted by the Examiner's notation to cache hardware (18A and 18B) as opposed to local memory. Accordingly, Applicant respectfully requests the Examiner remove the rejection of claims 1-25 and provide allowance of this application.

For the reasons outlined above, withdrawal of the rejection of record and an

allowance of this application are respectfully requested.

Respectfully submitted,

By: 

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